USN | | | | | | | | | | |

06EC63

Sixth Semester B.E. Degree Examination, Dec.2015/Jan.2016
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the different errors associated with an sample and hold circuit. **(05 Marks)**

b. Describe the terms INL and DNL for a DAC. **(05 Marks)**

c. Discuss the mixed signal layout strategy. **(05 Marks)**

d. A S/H circuit having the aperture uncertainty of 0.5 ns is used to sample a sinusoidal signal $v(t) = 2\sin 200\times10^3\pi t$. Find

i) Maximum sampling error.

ii) Maximum resolution of an ADC which uses the above S/H circuit, while maintaining a sampling error less than $\frac{1}{2}$ LSB. Assume $V_{ref} = 5V$. **(05 Marks)**

2 a. With a neat circuit diagram explain R-2R ladder DAC architecture. **(06 Marks)**

b. Design a 3 bit resistor-string ladder using a binary switch array. Assume that $V_{ref} = 5$ V and maximum power dissipation of the converter is 5 mw. Determine the value of analog voltage for each of the possible digital input codes. **(08 Marks)**

c. Discuss the advantages and disadvantages of using a dual slope versus a single slope ADC architecture. **(06 Marks)**

3 a. With a block diagram of the successive approximation ADC explain the successive approximation algorithm. **(08 Marks)**

b. Design a 3 bit charge scaling DAC and find the value of the output voltage for $D_2D_1D_0 = 010$ and 101. Assume $V_{ref} = 5$ V and C = 0.5 PF. **(06 Marks)**

c. With a block diagram describe pipeline ADC. **(06 Marks)**

4 a. Design a 3 bit current steering DAC using the generic current steering. Assume each current source I is of 5 μA find the total output current for each input code. **(06 Marks)**

b. Draw the CMOS analog multiplier and explain working. **(08 Marks)**

c. With a neat circuit diagram explain preamplification stage of comparator. **(06 Marks)**

PART – B

5 a. Explain the terms SNR and Interpolation. **(05 Marks)**

b. Write the time domain representation of $\frac{fs}{4}$ digital resonator and hence sketch its block level circuit diagram. **(05 Marks)**

c. With a neat block diagram, explain the accumulate and dump circuit used for decimation and averaging. Obtain the transfer function of the same. **(10 Marks)**

6 a. Explain Floating MOS capacitor and metal capacitors. **(10 Marks)**

b. With a neat sketches explain the typical CMOS process flow. Illustrate the differences between submicron process and other process flows. **(10 Marks)**

7 a. Explain the working of simple delay element using clocked CMOS logic. **(06 Marks)**

b. With a neat circuit diagram, explain the working of full adder bit implemented using dynamic logic and verify the operation of element as a 1 bit adder. **(08 Marks)**

c. Explain the working of synchronous up/down counter using an adder. **(06 Marks)**

8 a. With a circuit diagram, explain how common mode noise is eliminated to balance the output of an op-amp. **(06 Marks)**

b. Explain how a floating current source can be used to set the bias current of a push pull output stage. **(08 Marks)**

c. Explain how the addition of amplifiers to op-amp boost the gain and help slew rate. **(06 Marks)**

* * * * *